REMARKS

The applicants have carefully considered the official action dated August 11, 2004. In the official action, the examiner identified six patentably distinct inventions and required restriction of this application to one of those inventions. In particular, the examiner identified six groups of claims as follows: Group I (claims 1-4), Group II (claims 5-9), Group III (claims 10-12), Group IV (claims 13-15), Group V (claims 16-19), and Group VI (claims 20-22).

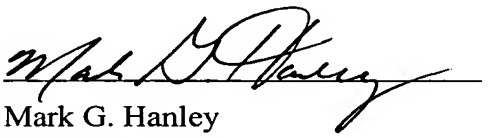
The applicants wish to thank the examiner for the telephonic interviews conducted on July 29, 2004, and September 16, 2004, during which the restriction requirement was discussed in detail. During the second interview, which was initiated by the applicants, the applicants submitted that due to the similarity of the subject matter recited in at least some of the identified groups of claims, it would not be an unreasonable burden for the examiner to conduct a search in connection with multiple ones of the identified groups of claims in this application. The examiner acknowledged that it may be reasonable to examine multiple groups of claims in this application and requested that the applicants file a response proposing groups for examination.

The applicants have carefully reviewed pending claims 1-22 in view of the above-noted groups of claims identified by the examiner. The applicants respectfully submit that due to similarities between claims 1-12 (Groups I, II, and III), it would not be a serious burden for the examiner to search the three sub-classes (i.e., 799, 724, and 704) identified by the examiner as pertaining to these claims. In particular, independent claim 1 is directed to a system for detecting bit errors, including a bit stream comparison unit and a multi-source agreement compliant electrical connector. Independent claim 5 is directed to a system for

determining a bit error rate of a device under test that, similar to the system recited in claim 1, includes a bit stream comparison unit and an electrical connector adapted to be coupled to a multi-source agreement compliant connection. The system recited in claim 5 also includes a bit stream generator and a processing unit that determines the bit error rate of the device under test. Additionally, independent claim 10, similar to claim 5, includes a bit stream generation circuit, a bit stream comparison circuit, and a multi-source agreement compliant electrical connector, and is generally configured to detect a bit error rate. The apparatus recited in claim 10 is embodied as a printed circuit assembly and is specifically configured to detect a bit error rate. The applicants submit that although the differences between claims 1, 5, and 10 may involve searching in three sub-classes (within the same class), no serious burden will be imposed on the examiner to conduct such a search and to examine claims 1-12 on the merits.

In view of the foregoing, the applicants respectfully request an early favorable action on the merits.

Respectfully submitted,



Mark G. Hanley
Reg. No. 44,736
Attorney for Applicants
Grossman & Flight, LLC
20 North Wacker Drive
Suite 4220
Chicago, Illinois 60606
312.580.1020

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Attorneys for Intel Corporation